



FIG. 1

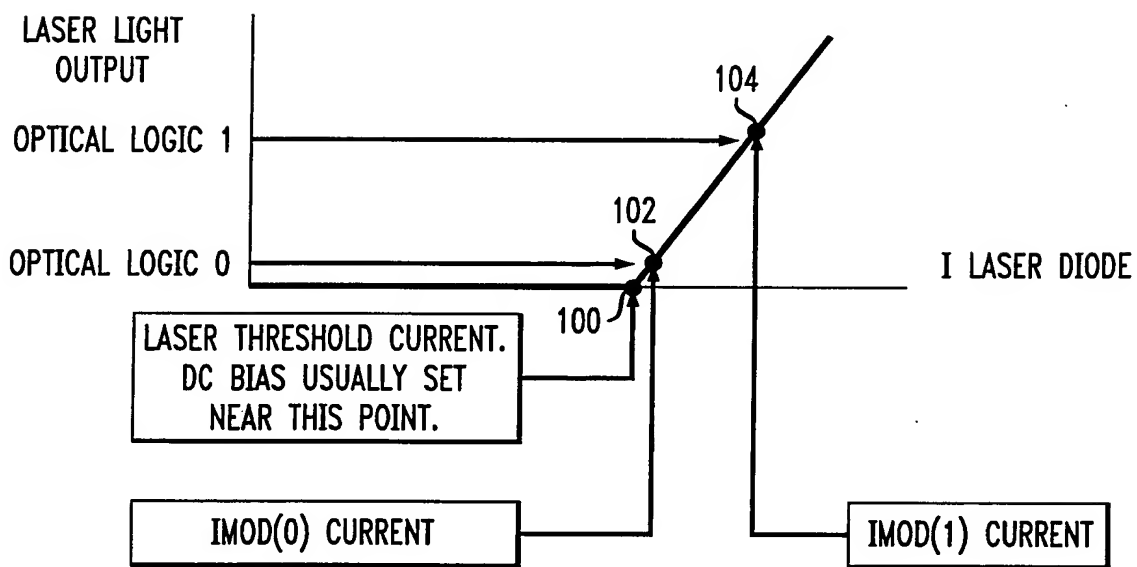
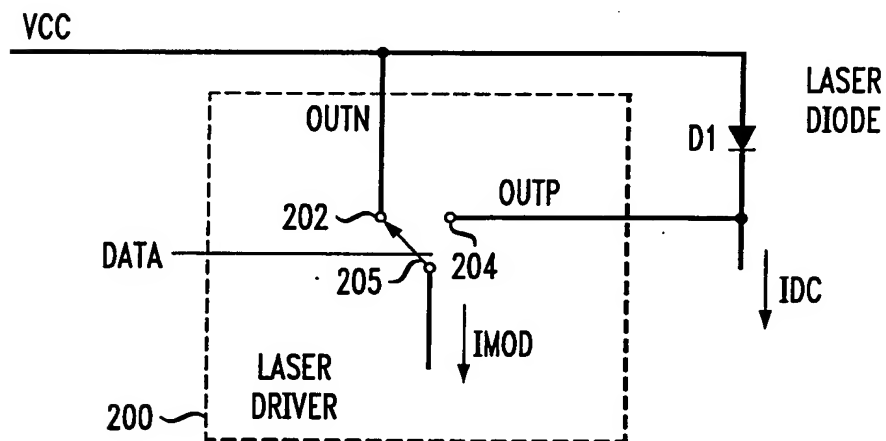
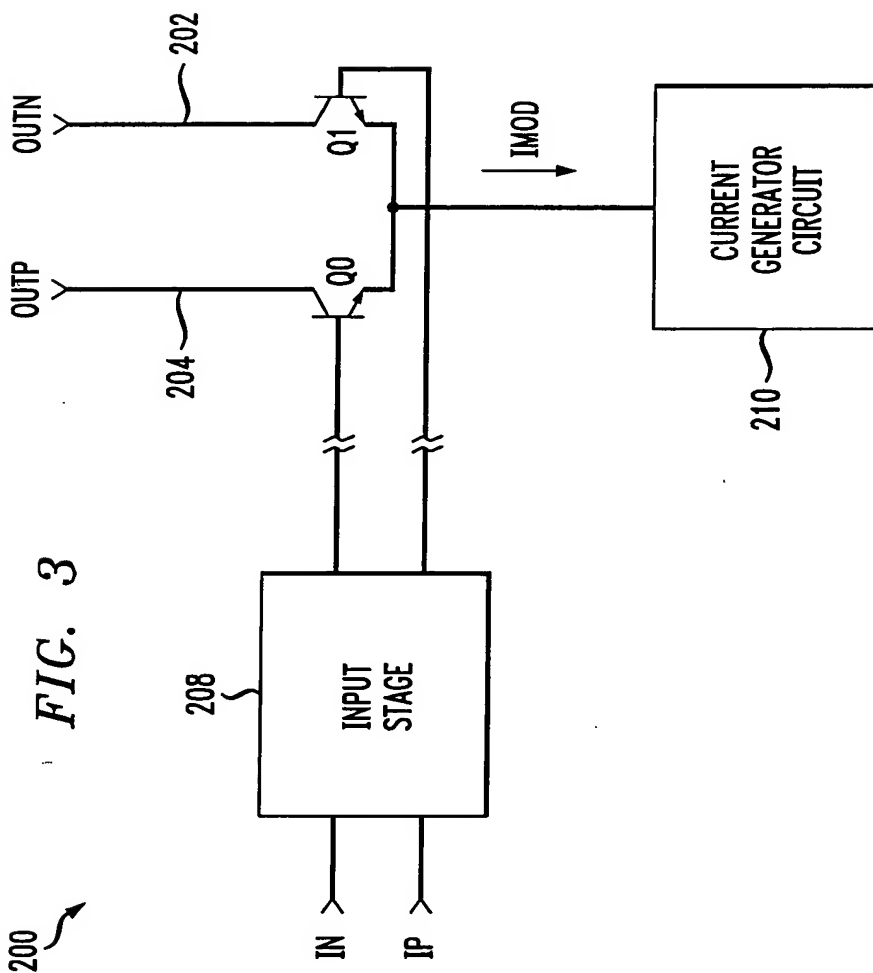
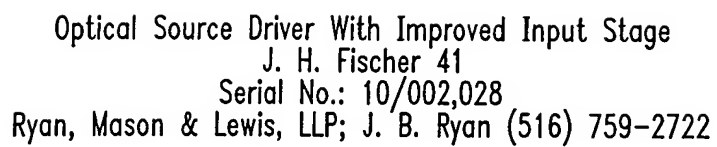


FIG. 2





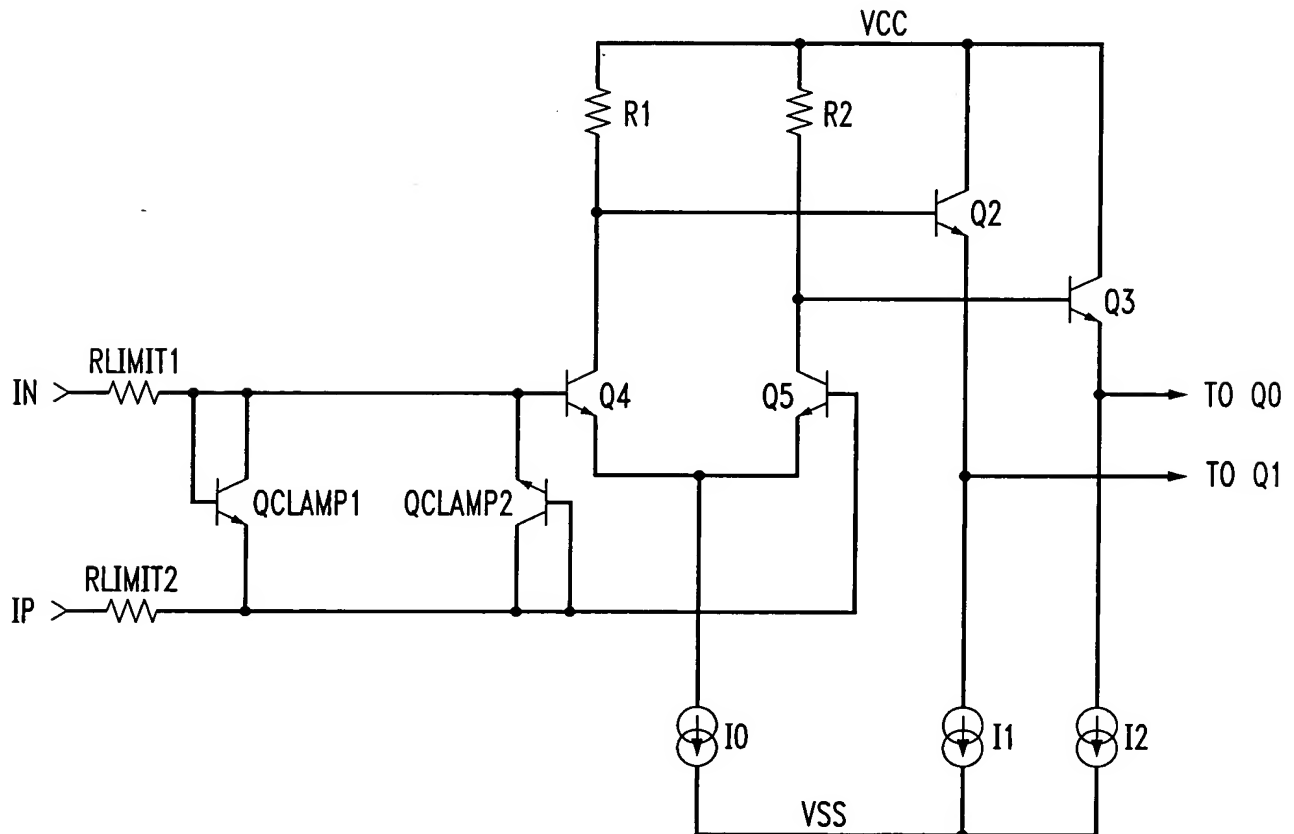


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The diagram shows a CMOS differential pair circuit. It consists of five transistors: Q1 and Q2 are PMOS devices, while Q3, Q4, and Q5 are NMOS devices. The PMOS transistors Q1 and Q2 have their gates connected to VDD and their sources connected to a common node. The NMOS transistors Q3 and Q4 have their gates connected to a common node and their sources connected to a common node. The NMOS transistor Q5 has its gate connected to the input signal IN and its source connected to the common node. The output signals are taken from the drains of Q1 and Q2, labeled TO Q0 and TO Q1. The input signal IP is connected to the gates of Q3 and Q4. The circuit is biased by current sources I0, I1, and I2, which are connected to the common nodes of the PMOS and NMOS transistors. The supply voltages are VDD and VSS.



FIG. 5
PRIOR ART



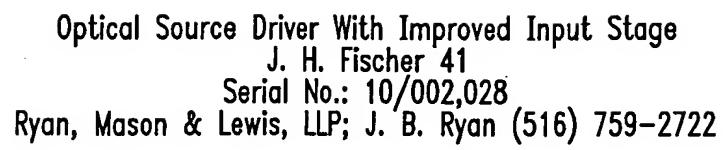


FIG. 6

